

## **REMARKS**

During a telephone conversation between the Examiner and Applicants' Attorney on March 12, 2007, the Examiner asserted that the limitation "*simultaneously* displaying said logic devices and said guard ring symbolically and schematically in a single display" (emphasis added) is not supported in Applicants' specification. Although Applicants' disagree with the Examiner's assertion, Applicants have removed the term "simultaneously" from the claims in order to speed prosecution.

Applicants have amended the claims to define "displaying said logic devices and said guard ring symbolically and schematically in a single integrated display", support for which can be found in paragraph 0020 of Applicants' specification. More specifically, Applicants' specification provides that the present invention also allows for designing of a guard ring structure with generated virtual design levels (eg., guard ring virtual level, I/O virtual level, ESD virtual level), allows for a graphical and schematic representation view of a guard ring structure, allows for designing of a guard ring structure symbology and symbol, and allows for designing of a guard ring structure symbology and symbol hierarchy which *integrates* the existing circuit design symbol view with the guard ring symbol view. The present invention allows for checking of a guard ring structure, and allows for verification of a guard ring structure.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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